Curriculum Vitae

Dr. Sarvesh Dubey

Assistant Professor (Physics)

Dept. of Physics, L.N.D. College,Motihari,

(A Constituent Unit of B.R. Ambedkar Bihar University, Muzaffarpur) Bihar

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Google Scholar: https://scholar.google.com/citations?user=JW6hR_gAAAAJ&hl=en

Mendeley: https://www.mendeley.com/profiles/sarvesh-dubey2/?viewAsOther=true

Scopus: https://www.scopus.com/authid/detail.uri?authorId=55417259600

Academic Qualifications:

Exam/Degree	Board/University	Year	Subjects (Specialization)	%	Division
Ph.D.	Indian Institute of Technology (BHU), Varanasi	2012	Physics	Awarded	
M.Sc.	U.P. Autonomous P.G. College, Varanasi (V.B.S. Purvanchal University, Jaunpur)	2006	Physics (Speclz. Electronics)	68.3	First
B.Sc.	U.P. Autonomous P.G. College, Varanasi (V.B.S. Purvanchal University, Jaunpur)	2004	Physics, Mathematics	69.4	First
12^{th}	U.P. Board Allahabad	2001	Mathematics Group	63.8	First
10^{th}	U.P. Board Allahabad	1999	Science Group	72	First
NET	U.G.C.	July-2016	Electronic Science		
GATE (Graduate Aptitude Test in Engineering)		2008 2007	Physics	AIR-201 97.7 Percentile	

Area of Interests

- Modeling, TCAD Simulation, Microelectronics, Nanoelectronics, Tunnel FET,Semiconductor Devices and Physics,Quantum Mechanics, Metaphysics

Fellowships/Awards/Honors/Recognition

- Session Co-chair at IEEE International Conference on Cutting-edge Technologies in Engineering (ICon-CuTE) 2019 at SRM University, Lucknow
- Enlisted three times in the *Golden List of Reviewers for IEEE Trans. on Electron Devices*, December **2019, 2016 and 2015**
- Reviewer of some International Journals
  - IEEE Trans. on Electron Devices
  - Solid State Electronics (Elsevier)
  - IEEE Sensors
  - Superlattices and Microstructures (Elsevier)
  - Microelectronics Journal (Elsevier)
  - SILICON (Springer)
- U.G.C. Senior Research Fellowship (**SRF**) & Junior Research Fellowship (**JRF**)at IIT(BHU), Varanasi

Academic Projects

1. PhD Thesis Title: *Analytical Modeling and Simulation of Short-ChannelDouble-Gate(DG) MOSFETs with a Vertical Gaussian-Like Doping Profile*(Supervisor:Prof. Satyabrata Jit)

Validation Tools:ATLAS™ (2-D Device Simulator from SILVACO Int., Singapore), MATLAB

2. e-Content Development Project: Co-Ordinator, e-Content development project at L.N.D. College, Motihari(Constituent Unit of Bhimrao Ambedkar Bihar University, Muzaffarpur).

3. e-Content Creation: Member and creator of the committee for creation of e-contents of B.Sc. (Hons.) Physics and M.Sc. Physics syllabus at L.N.D. College Motihari(Constituent Unit of Bhimrao Ambedkar Bihar University, Muzaffarpur).

Working Experience

- ✓ Worked as Assistant Professor in Shri Ramswaroop Memorial University, Lucknow-Deva Road Barabanki-225003from July 18, 2013 to August 30, 2017 at the Faculty of Electronics and Communication Engineering.
- ✓ Presently working as Assistant Professor (Physics) at L.N.D. College Motihari (A Constituent unit of B.R. Ambedkar Bihar University, Muzaffarpur) (NAAC Accredited B+) since September 01, 2017.

Details of B.Tech. Research project completed under my guidance

1. "GSM Based Car Security System" S. R. A. Naqvi (201210104110711) and Akash Tiwari (201210104110702)

Details of M.Tech. Research project completed under my guidance

1. "Diagnosis of Sleep Disorder using Short Time Frequency Analysis of PSD Applied on EEG Signals (ROC-LOC) Channels" by Varsha Pandey (201310104010003) (August 2015).
2. "Performance Analysis of IDMA Scheme using High Girth Quasi-Cyclic LDPC Codes" by Anurag Saxena (201310104010004) (June 2015).

Details of Ph.D. being going on under my guidance in SRMU

1. Modeling and Simulation of Nanoscale Tunnel FETs by Rahul Misra.

2. Analysis and Investigations on Some NC FETs for low power applications by Er. Ravi Rastogi (Scientist, NIELIT, Gorakhpur)

Administrative Experience

- Course-Coordinator, B.C.A., L.N.D. College Motihari (NAAC Accredited B+).
- Member, IQAC, LND College, Motihari
- Member, Purchasing Committee, LND College, Motihari
- Member, Development Committee, LND College, Motihari
- ACS in various University level Exams, LND College Motihari
- In-Charge, Virtual Classrooms at L.N.D. College Motihari
- Coordinator, Remedial Coaching for Entry-in Services, L.N.D. College, Motihari.
- In-charge,Language-Lab, L.N.D. College, Motihari.
- Professor-in-Charge, Implementation National Innovation and Start-up Policy (NISP), Ministry of Education at LND College Motihari.

Personal Details

Father's Name: Dr. Krishna Chandra Dubey (Professor)
Mother's Name: Smt. Kanchan Dubey

Sex	:	Male
Marital Status	:	Married
Nationality	:	Indian
Permanent Address	:	Varanasi, U.P., India
Date of Birth	:	September, 16.

Place: Motihari (**Sarvesh Dubey)**

Publications

Book Chapter

1. Pramod Kumar Tiwari, **Sarvesh Dubey** and S. Jit, "Double-Gate (DG) MOSFETs: A Review", Advances in Microelectronics and Photonics, **Nova Science Publishers Inc., New York (ISBN: 978-1-61470-956-5),** pp. 61-124, **2012**.
2. Ved Prakash Dubey, Devendra Kumar, **Sarvesh Dubey**, A Modified Computational Scheme and Convergence Analysis for Fractional Order Hepatitis E Virus Model, *In book*: **Advanced Numerical Methods for Differential Equations: Applications in Science and Engineering**, 279-312, 2021, CRC Press,Taylor & Francis Group, Boca Raton, Florida, U.S.A.(ISBN-9780367473112) DOI: 10.1201/9781003097938-11**.**

Articles Published in International Journals (*Total Impact Factor Points* >80)

3. Ved Prakash Dubey, Jagdev Singh, Ahmed Mohammed Alshehri, **Sarvesh Dubey**. Devendra Kumar, "A Comparative Analysis of Two Computational Schemes for Solving Local Fractional Laplace Equations" **Mathematical Methods in the Applied Sciences**, pp. 1-20, 2021, WoS & Scopus, Elsevier-SCI, DOI: https://doi.org/10.1002/mma.7642, **IF: 2.321** (ISSN-1099-1476)
4. Nitish Kumar, V. Purwar, H. Awasthi, Rajeev Gupta, K. Singh & **Sarvesh Dubey,** "Modeling the threshold voltage of core-and-outer gates of ultra-thin nanotube Junctionless-double gate-all-around (NJL-DGAA) MOSFETs" **Microelectronics Journal *(Elsevier)*, 113, pp. 105104,**https://doi.org/10.1016/j.mejo.2021.105104 , **July 2021, [ISSN: 0026-2692,SCI, Impact Factor:1.605**].
5. Nitish Kumar, H. Awasthi, V. Purwar, Abhinav Gupta & **Sarvesh Dubey,** "Impact of Temperature Variation on Analog, Hot-Carrier Injection and Linearity Parameters of Nanotube Junctionless Double-Gate-All-Around (NJL-DGAA) MOSFETs" ***Silicon*** (***Springer***), https://doi.org/10.1007/s12633-021-01069-5, March **2021 [ISSN: 1876-9918,SCI, Impact Factor:2.670**.]
6. Rahul Misra, Kunal Singh, Mirgender Kumar, Ravi Rastogi, Arun Kumar and **Sarvesh Dubey,** "An Ultra-Low-Power Black Phosphorus (B-Ph)/Si Heterojunction Dopingless-Tunnel FET (HD-TFET) with Enhanced Electrical Characteristics", **Superlattices and Microstructures *(Elsevier)***(ISSN: 0749-6036)**,** Vol. 149, pp: 106752**, 2021[*SCI*, Impact Factor:2.658].**
7. V. P. Dubey, **Sarvesh Dubey**, D Kumar, J. Singh, "A Computational Study of Fractional Model of Atmospheric Dynamics of Carbon Dioxide Gas", **Chaos, Solitons and Fractals (ELSEVIER)** (ISSN: 0960-0779), Volume 142, 110375, January **2021[*SCI*, Impact Factor:3.764]**.
8. Vaibhav Purwar, Rajeev Gupta, Nitish Kumar, Himanshi Awasthi, V K Dixit, Kunal Singh, **Sarvesh Dubey,** Pramod Kumar Tiwari, "Investigating linearity and effect of temperature variation on analog/RF performance of dielectric pocket high-k double gate-all-around (DP-DGAA) MOSFETs", **Applied Physics A(*Springer*)** (ISSN: 1432-0630) 126:746, **(2020)** [**SCI, Impact Factor:1.810].**

9. Himanshi Awasthi, Nitish Kumar, Vaibhav Purwar, Rajeev Gupta, and **Sarvesh Dubey**, "Impact of Temperature on Analog/RF Performance of Dielectric Pocket Gate-All-Around (DPGAA) MOSFETs" ***Silicon*** (***Springer***), https://doi.org/10.1007/s12633-020-00610-2(July **2020**),**SCI, Impact Factor:1.5**.

10. Vijay Kumar Dixit, Rajeev Gupta, PSTN Srinivas and **Sarvesh Dubey**, "Back Bias Induced Modeling of Subthreshold Characteristics of SOI Junctionless Field Effect Transistor (JLFET)" ***Silicon*** (***Springer***),https://doi.org/10.1007/s12633-020-00590-3(July **2020**) **SCI, Impact Factor:1.5**

11. Vijay Kumar Dixit, Rajeev Gupta, Vaibhav Purwar, PSTN Srinivas, **Sarvesh Dubey**, "Effect of Substrate Induced Surface Potential (SISP) on Threshold Voltage of SOI Junction-Less Field Effect Transistor (JLFET)" ***Silicon*** (***Springer***), 12, pages-921–926 (**2020**) **SCI, Impact Factor:1.5**

12. Kunal Singh, S Kumar, PK Tiwari, AB Yadav, **Sarvesh Dubey**, S Jit, "Semianalytical Threshold Voltage Model of a Double-Gate Nanoscale RingFET for Terahertz Applications in Radiation-Hardened (Rad-Hard) Environments", ***Journal of Electronic Materials*** (***Springer***), Volume 48, Issue 10, pp 6366-71, **Oct2019[ISSN No. 1543-186X, SCI, I.F.:1.774]**.

13. A. Kumar, **Sarvesh Dubey**, P. K. Tiwari "Threshold Voltage Modeling of Double Gate-All-Around Metal-Oxide-Semiconductor Field-Effect-Transistors (DGAA MOSFETs) Including the Fringing Field Effects", ***Journal of Nanoelectronics and Optoelectronics*** (American Scientific Publi)**,** Vol. 14 (11), pp. 1555-1564, **2019** [**SCI, I.F. 1.069**].

14. M. Kumar, V. P. Singh, **Sarvesh Dubey**, Y Suh, Si-Hyun Park, "GaN Nanophosphors for White-light Applications",***Optical Materials*** (***Elsvier***), Volume 75, pp 61–67, **Jan2018[ISSN No. 09253467, SCI, Impact Factor:3.08]**.

15. M. Kumar, **Sarvesh Dubey**, Vanga Rajendar, Si-Hyun Park, "Fabrication of ZnO Thin Films by Sol–Gel Spin Coating and Their UV and White-Light Emission Properties",***Journal of Electronic Materials*** (***Springer***), Volume 46, Issue 10, pp 6029–6037, **May2017[ISSN No. 1543-186X, SCI, Impact Factor:1.774]**.

16. Kunal Singh, S. Kumar, E. Goel, **Sarvesh Dubey,** S. Jit, "Effects of Elevated Source/Drain and Side Spacer Dielectric on the Drivability Optimization of Non-Abrupt Ultra Shallow Junction Gate Underlap DG MOSFETs",***Journal of Electronic Materials*** (***Springer***), Vol. 46, Issue 1,pp.520-526,**January2017**, [**ISSN No. 1543-186X, SCI, Impact Factor:1.774**].

17. Kunal Singh, S. Kumar, E. Goel, **Sarvesh Dubey,** S. Jit, "Subthreshold Current and Swing Modeling of Gate Underlap DG MOSFETs with Source/Drain Lateral Gaussian Doping Profile", ***Journal of Electronic Materials*** (***Springer***), Vol. 46, Issue 1,pp.579-586,**January2017[ISSN No. 1543-186X, SCI, Impact Factor:1.774].**

18. P. K. Tiwari, V. R. Samoju, Thandva Sunkara, **Sarvesh Dubey,** S. Jit , "Analytical Modeling of Threshold Voltage for Symmetrical Silicon Nano-Tube Field-Effect-Transistors (Si-NT FETs)", ***Journal of Computational Electronics (Springer)***,Vol. 15pp.516-24,**2016**[***SCI,* I. F. 1.532**].

19. Kunal Singh, M. Kumar, **Sarvesh Dubey,** S. Kumar, S. Jit, "Analytical Modeling of Potential Distribution and Threshold Voltage of Gate Underlap DG MOSFETs with a Source/Drain Lateral Gaussian Doping Profile", ***Journal of Electronic Materials*** (***Springer***), Vol. 45, Issue 4,pp.2184-2192,**2016** [***SCI,* I. F. 1.774**].

20. Gopi Krishna Saramekala, **Sarvesh Dubey,** Pramod Kumar Tiwari, "A threshold voltage model of short-channel fully-depleted (FD) recessed-source/drain (Re-S/D) SOI MOSFETs with high-K dielectric", ***Chinese Physics B*** (***IOP***), Vol. 24 No. 10pp.108505, **2015** [***SCI,* I. F. 1.223**].

21. Visweswara Rao Samoju, **Sarvesh Dubey**, Pramod Kumar Tiwari, Quasi-3D subthreshold current and subthreshold swing models of Dual-Metal Quadruple-Gate (DMQG) MOSFETs, ***Journal of Computational Electronics (Springer)***,Vol. 14pp.582-92,**2015**[***SCI,* I. F. 1.532**].

22. Gopi Krishna Saramekala, **Sarvesh Dubey** and Pramod Kumar Tiwari, "Analog and radio-frequency (RF) performance evaluation of fully-depleted (FD) recessed source/drain (Re-S/D) SOI MOSFETs", ***Supperlattices and Microstructures (Elsevier),*** Vol. 76 (8), pp: 77-89**, 2014 [*SCI*, *Impact Factor*:2.120].**

23. Gopi Krishna Saramekala, Abirmoya Santra, Mirgender Kumar, **Sarvesh Dubey**, Satyabrata Jit and Pramod Kumar Tiwari, "Analytical subthreshold current and subthreshold swing models of short-channel dual-metal-gate (DMG) fully-depleted recessed-source/drain (Re-S/D) SOI MOSFETs", ***Journal of Computational Electronics (Springer)***, Vol. **13**, pp 467-76-28, **2014 [*SCI, Impact Factor.*:1.532].**

24. Gopal Rawat, Ekta Goel, Sanjay Kumar, Mirgender Kumar, **Sarvesh Dubey**, and S. Jit, "Analytical Modeling of Threshold Voltage of Ion-Implanted Strained-Si-on-Insulator (SSOI) MOSFETs", ***Journal of Nanoelectronics and Optoelectronics (ASP)*** Vol. 9, pp. 442-448, **2014 (*SCI, Impact Factor.*:1.069).**

25. Pramod Kumar Tiwari, Gopi Krishna Saramekala, **Sarvesh Dubey** and Anand Kumar Mukhopadhyay, "An analytical model for the subthreshold current and subthreshold swing of short-channel double-material-gate MOSFETs with a strained-silicon channel on silicon-germanium substrates", ***Journal of Semiconductors (IOP)***, Vol. **35**, Issue 10,104002-7, **2014 (ESCI)**

26. Gopal Rawat, Sanjay Kumar, Ekta Goel, Mirgender Kumar, Sarvesh Dubey, and S. Jit, "Analytical modeling of subthreshold current and subthreshold swing of Gaussian doped (GD) strained-Si-on-insulator (SSOI) MOSFETs,***Journal of Semiconductors (IOP)***, Vol. **35**, Issue 8,084001-8, **2014 (ESCI).**

27. Abirmoya Santra, Mirgender Kumar, **Sarvesh Dubey**, Satyabrata Jit and Pramod Kumar Tiwari, Analytical modeling of threshold voltage of stacked Triple-Material-Gate (TMG) Strained-Si (s-Si) on Silicon-Germanium-on-Insulator (SGOI) MOSFETs, accepted for publication in ***Journal of Active and Passive Electronic Devices*** (ISSN: 1555-0281(print), ISSN: 1555-029X (online).

28. Sarvesh Dubey, Abirmoya Santra, Santunu Sarangi, Shiv Bhushan, Gopi Krishna S., Mirgender Kumar and Pramod Kumar Tiwari, An Analytical Threshold Voltage Model for Triple-Material Cylindrical Gate-All-Around (TM-CGAA) MOSFETs, ***IEEE Transactions on Nanotechnology***, Vol. 12 (5), pp.1-9, **2013 [*SCI*, *Impact Factor*:2.2)]**.

29. Mirgender Kumar, **Sarvesh Dubey**, Pramod Kumar Tiwari and S. Jit, "Analytical Modeling and Simulation of Subthreshold Characteristics of Back-Gated SSGOI and SSOI MOSFETs: A

Comparative Study," ***Current Applied Physics (Elsevier)***,Vol. 13 (8), pp. 1778-86,**2013[*SCI*, *Impact Factor*:2.281)]**.

30. Gopi Krishna S., Abirmoya Santra, **Sarvesh Dubey**, Satyabrata Jit, Pramod Kumar Tiwari**,** An analytical threshold voltage model for a short-channel dual-metal-gate (DMG) recessed-source/drain (Re-S/D) SOI MOSFET, ***Supperlattices and Microstructures (Elsevier),*** Vol. 60 (8), pp:580-595**, 2013 [*SCI*, *Impact Factor*:2.120].**
31. Santunu Sarangi, Shiv Bhushan, Abirmoya Santra, Sarvesh Dubey, Satyabrata Jit and **Pramod Kumar Tiwari**, A rigorous simulation based study of gate misalignment effects in gate engineered double-gate (DG) MOSFETs, ***Supperlattices and Microstructures (Elsevier),*** Vol. 60 (8), 263-279,**2013 [*SCI*, *Impact Factor*:2.120].**
32. Shiv Bhushan, Santunu Sarangi, Abirmoya Santra, Gopi Krishna S, **Sarvesh Dubey**, P.K. Tiwari, An Analytical Model for the Threshold Voltage of Short-Channel Double-Material-Gate (DMG) MOSFETs with a Strained-Si (s-Si) Channel on Silicon-Germanium (SiGe) Substrates, ***Journal of Semiconductor Technology and Sciences (Institute of Electronics Engineers of Korea)*** **(**Impact Factor: 0.8), Vol. 13, No. 4, pp. 367-380, **2013[*SCI*, *Impact Factor*:0.8]**.
33. Mirgender Kumar, **Sarvesh Dubey**, Pramod Kumar Tiwari, and S. Jit, "Analytical Models of Subthreshold Current and Swing of Short-Channel Strained-Si (s-Si) on Silicon-Germanium-on-Insulator (SGOI) MOSFETs", ***Superlattices and Microstructures (Elsevier)*****,** Vol. 58, pp: 1-10,**2013 [*SCI*, *Impact Factor*:2.120]**.
34. Mirgender Kumar, **Sarvesh Dubey**, Pramod Kumar Tiwari, and S. Jit, "Two-Dimensional Modeling of Subthreshold Current and Subthreshold Swing of Double-Material-Gate (DMG) Strained-Si (s-Si) on SGOI MOSFETs", ***Journal of Computational Electronics (Springer)***,Vol. **12 (2)**, pp 275-280, **2013 [*SCI*, *Impact Factor*:1.532]**.
35. **Sarvesh Dubey,** Pramod Kumar Tiwari and S. Jit, "On-Current Modeling of Short- Channel Double-Gate (DG) MOSFETs with a Vertical Gaussian-like Doping Profile" ***Journal of Semiconductors (IOP)***, Vol. **34**, Issue 5,054001, **2013 (ESCI)**.
36. Mirgender Kumar, **Sarvesh Dubey**, Pramod Kumar Tiwari and S. Jit, "Analytical Modeling of Threshold Voltage of Short-Channel Strained-Si on Silicon-Germanium-on-Insulator (SGOI) MOSFETs with Localized Charges," ***Journal of Computational and Theoretical Nanoscience (ASP)***, Vol. **11**, Issue 1,pp.165-172, **2014[*SCI*, *Impact Factor*:1.665]**.
37. Mirgender Kumar, **Sarvesh Dubey**, Pramod Kumar Tiwari and S. Jit, "An Analytical Model of Threshold Voltage for Short-Channel Double-Material-Gate (DMG) Strained-Si (s-Si) on Silicon-Germanium-on-Insulator (SGOI) MOSFETs", ***Journal of Computational Electronics (Springer)***, Vol. **12**, pp 20-28, **2013 [*SCI*, *Impact Factor*:1.532]**.
38. Shiv Bhushan, Santunu Sarangi, Abirmoya Santra, Mirgender Kumar, **Sarvesh Dubey**, S. Jit and P. K. Tiwari, "An Analytical Surface Potential Model for Strained-Si on Silicon-Germanium MOSFET Including the Effects of Interface Charges," ***Journal of Electron Devices***, Vol. **15**, pp. 1285-1290, **2012**.
39. Pramod Kumar Tiwari, **Sarvesh Dubey**, Kunal Singh, and S. Jit, "Analytical modeling of subthreshold current and subthreshold swing of short-channel triple-material double-gate (TM-DG) MOSFETs," ***Superlattices and Microstructures (Elsevier)***,Vol. **51**, pp. 715-724, **2012 [*SCI*, *Impact Factor*:2.120]**.
40. Pramod Kumar Tiwari, **Sarvesh Dubey** and S. Jit, "A Doping dependent threshold voltage model of uniformly doped short-channel symmetric double-gate (DG) MOSFETs", ***Journal of Nano-***

and Electronic Physics (Sumy State University, Ukraine), Vol. **3**, pp. 963-971, **2011 (SCOPUS)**.

41. **Sarvesh Dubey**, Dheeraj Gupta, Pramod Kumar Tiwari, and S. Jit, "Two-Dimensional Analytical Modeling of Threshold Voltage of Doped Short-Channel Triple-Material Double-Gate (TM-DG) MOSFETs", ***Journal of Nano- and Electronic Physics (Sumy State University, Ukraine)*****,** Vol. **3**, pp. 576-583, **2011 (SCOPUS)**.
42. **Sarvesh Dubey**, Pramod Kumar Tiwari and S. Jit, "A 2D model for the subthreshold swing of short-channel double-gate (DG) MOSFETs with a vertical Gaussian-like doping profile", ***Journal of Applied Physics (AIP),*** Vol. **109,** Issue 5, pp. 054508, **2011 [*SCI*, *Impact Factor*:2.286]**.
43. **Sarvesh Dubey**, Pramod Kumar Tiwari and S. Jit, "A 2D Model for the Potential Distribution and Subthreshold Current of Short-Channel Double-Gate (DG) MOSFETs with a Vertical Gaussian-Like Doping Profile", ***Journal of Nanoelectronics and Optoelectronics (ASP),*** Vol. **5**, Issue 3, pp. 332-339, **2010 (*SCI, Impact Factor.*:1.069)**.
44. Pramod Kumar Tiwari**, Sarvesh Dubey**, M. Singh and S. Jit, "A two-dimensional Analytical Model for Threshold Voltage of Short-channel Triple-material Double Gate (TM-DG) MOSFETs", ***Journal of Applied Physics (AIP),*** Vol. **108**, Issue 7, 074508, **2010 [*SCI*, *Impact Factor*:2.286]**.
45. **Sarvesh Dubey**, Pramod Kumar Tiwari and S. Jit, "A 2D Model for the Potential Distribution and Threshold Voltage of Short-Channel Double-Gate (DG) MOSFETs with a Vertical Gaussian-Like Doping Profile, ***Journal of Applied Physics (AIP),*** Vol. **108**, Issue 3, 034518, **2010 [*SCI*, *Impact Factor*:2.286]**.

<u>Articles Published/Presented and Talks in International/National Conferences</u>

46. Participated in Refresher Course in Physics at UGC, HRD Centre, University of Lucknow from Feb.12, 2021 to Feb.27, 2021. Secured A+ grade.
47. Participated in 85th Orientation Course at UGC, HRD Centre, Banaras Hindu University from Jan.25, 2020 to Feb.14, 2021. Secured A grade.
48. Mirgender Kumar, Vivek Mishra, Rahul Misra, **Sarvesh Dubey**, "Investigating the Possibility to Extend Planar Technology to 10 nm Scale with UTBB DMG SSOI MOSFETs"2019/11/14 Conference **2019**International Conference on Cutting-edge Technologies in Engineering (ICon-CuTE) Pages 63-68 ***@ IEEE conference proceeding.***
49. **Sarvesh Dubey,** "Revisiting Carrier Transport in Nano-transistors", delivered **Invited Talk**,in***TQIP,*** **Dept. of Electrical Engineering at IIT Patna, India, July 8, 2018.**
50. **Sarvesh Dubey,** "Aspects of Carrier Transport in Nano-transistors", delivered **Invited Talk**,in***National Conference on advances and innovations in Electrical and Electronics Engineering (AIEECE-2016)*** **at Poornima University, Jaipur, India, November 16-17, 2016.**
51. **Sarvesh Dubey**, Anand Mukhopadhyay and Pramod K. Tiwari, "Effect of Temperature Variation on the Characteristics of Dual-Metal Gate Strained Silicon on Si1-XGeX Substrate MOSFET", in ***International Symposium on Semiconductor Materials and Devices (ISSMD-2015) at Anna University, Chennai,*** **February 02-05, 2015.**

52. Ekta Goel, Mirgender Kumar, **Sarvesh Dubey** and S. Jit, A Threshold Voltage Model of High-k Gate Stack Short-Channel Double-Gate (DG) MOSFETs, *National Conference on Nanoscience and Instrumentation Technology, **NIT Kurukshetra**,* **March 2013**.

53. Sanjay Kumar, Mirgender Kumar, **Sarvesh Dubey** and S. Jit An Analytical Modeling of Surface Potential and Threshold Voltage of Non-uniformly Doped Double-Gate (DG) MOSFETs, *National Conference on Nanoscience and Instrumentation Technology, **NIT Kurukshetra**,* **March 2013**

54. Shiv Bhushan, Santunu Sarangi, Abirmoya Santra, Gopi Krishna S, **Sarvesh Dubey**, P.K. Tiwari, An Analytical Surface Potential Modeling of Fully-Depleted Symmetrical Double-Gate (DG) Strained-Si MOSFETs Including the Effect of Interface Charges, *2nd Student's Conference in Engineering and Systems*, MNNIT Allahabad, **2013**.

55. Mirgender Kumar, **Sarvesh Dubey**, Pramod Kumar Tiwari, S. Jit, A Comparative Study of Short-Channel-Effects of strained-Si on Insulator (SSOI) and strained-Si on Silicon-Germanium-on-Insulator (SSGOI) MOSFETs, in *International Conference on Electrical and Electronics Engineering (ICEEE-2013),accepted for **@WCE conference proceeding,***London, July 04-06, **2013**.

56. Mirgender Kumar, **Sarvesh Dubey**, Pramod Kumar Tiwari, and S. Jit, "Back Gated (BG) Strained-Si-on-Silicon-Germanium-on-Insulator (SSGOI) MOSFETs for Improved Switching Speed and Short-Channel-Effects (SCEs)", in *international conference on Recent Trends in Applied Physics and Material Science, accepted for **@AIP conference proceeding***, Bikaner, Feb 01-03, **2013**.

57. Mirgender Kumar, **Sarvesh Dubey**, Pramod Kumar Tiwari, and S. Jit, "Quantitative Performance Investigations of Back Gated Strained-Si-on-Insulator (SSOI) MOSFETs: Towards Double-Gate (DG) Operation", in *international conference on Nanoelectronics and Nano devices (ICNEND)*, *accepted for**@SNEM conference proceeding,*** Chennai, Jan. 21-22, **2013**.

58. Mirgender Kumar, **Sarvesh Dubey,** P. K. Tiwari and S. Jit, "A 2D Analytical Modeling Approach for Nanoscale Strained-Si (s-Si) on Silicon-Germinium-on-Insulator (SGOI) MOSFETs by Evanescent Mode Analysis", in *International Conference on Communications, Devices and Intelligent Systems (CODIS),*pp.469-472 ***@ IEEE conference proceeding,*** Calcutta, December 28-29, **2012**.

59. Mirgender Kumar, **Sarvesh Dubey,** P. K. Tiwari and S. Jit, "An Analytical Modeling of Interface Charge Induced Effects on Subthreshold Current and Subthreshold Swing of strained-Si (s-Si) on Silicon-Germinium-on-Insulator (SGOI) MOSFETs", in *International Conference on Computers and Devices for Communication(CODEC) **@ IEEE conference proceeding,*** Calcutta, December 17-19, **2012**.

60. Mirgender Kumar,**Sarvesh Dubey**, Pramod Kumar Tiwari and S. Jit, "Analytical Study of Interface Charges Effect on Short Channel Effect of Strained-Si on Silicon-Germanium-on-Insulator (SGOI) MOSFETs", in *International Conference on Quantum, Nano and Micro Technologies* (*ICQNM),**©IARIA conference proceeding,* Rome, August 19 - 24, **2012**.

61. Mirgender Kumar, **Sarvesh Dubey,** P. K. Tiwari and **S. Jit**, "Analytical Modeling and ATLAS Based Simulation of the Surface Potential of Double-Material-Gate Strained-Si on Silicon-on-Germanium-on-Insulator (DMG-SGOI) MOSFETs" *in Proc. IEEE International Conference on Multimedia, Signal Processing and Communication Technologies* (**IMPACT-2011**), pp. 228-231 (December 17-19, **2011** at **AMU, Aligarh**).

62. A. Santra, **Sarvesh Dubey**, Mirgender Kumar, Pramod Kumar Tiwari and **S. Jit** "An Analytical Study of the Effect of Interface Charges on the Surface Potential of Strained-Si on Silicon-Germanium-on-Insulator (SGOI) MOSFETs" *in Proc. National Conference on Emerging Trends in Electrical and Electronics Engineering (ETEEE-2011)* pp.56-57(November 26-27, **2011** at **K.N.I.T., Sultanpur**).

63. Mirgender Kumar,**Sarvesh Dubey,** P. K. Tiwari and **S. Jit**, "Extremely Scaled EOT Bi-Layered High-k stacked Double-Material Double-gate Strained-Si MOSFET for High Performance Band-Edge (BE) CMOS Technology" *in Proc. National symposium on Recent Advances in Nanosciences, Engineering & Technology (RANET-2011)* pp. 76 (November 19-20, **2011** at **ABV-IIITM, Gwalior**).

64. Pramod Kumar Tiwari, **Sarvesh Dubey** and S. Jit, "A Doping dependent threshold voltage model of uniformly doped short-channel symmetric double-gate (DG) MOSFETs", presented in poster section in International symposium on semiconductor materials and devices (**ISSMD**), M. S. University, **Vadodara**, **2011**.

65. **Sarvesh Dubey**, Dheeraj Gupta, Pramod Kumar Tiwari, and S. Jit, "Two-Dimensional Analytical Modeling of Threshold Voltage of Doped Short-Channel Triple-Material Double-Gate (TM-DG) MOSFETs", presented in poster section in International symposium on semiconductor materials and devices (**ISSMD**), M. S. University, **Vadodara, 2011**.

66. Pramod Kumar Tiwari**, Sarvesh Dubey**, M. Singh and S. Jit, "An analytical subthreshold current model for triple-material double-gate (TM-DG) MOSFETs", published in the procd. of International Conference on Electronic Systems (**ICES)**, **NIT-Rourkela**, pp.143-145, **2011**.

67. Pramod Kumar Tiwari, **Sarvesh Dubey** and S. Jit, "Subthreshold swing model for asymmetric 3T double-gate (DG) MOSFETs" published in the procd. of 10th IEEE International Conference on Solid-State and Integrated Circuit Technology (**ICSICT), Shanghai,China**, pp.1796-1798, **2010**.

68. Pramod Kumar Tiwari, **Sarvesh Dubey** and S. Jit, "Subthreshold current model for short-channel double-gate (DG) MOSFETs with vertical Gaussian doping profile", published in the procd. of the Latest Trends on Circuits System and Signal, **Greece,** pp. 27-34, **2010**.

69. **Sarvesh Dubey**, Pramod Kumar Tiwariand S. Jit," Surface potential model for Gaussian doped DG MOSFET", published in the procd. of International Workshop on Physics of Semiconductor Devices (**IWPSD), DRDO-J.M.I.New Delhi**, pp. 751-754, **2009.**